IN THE SPECIFICATION

Please replace Paragraph No. 54 (page 12) with the following:

[0054] Figure 6 shows tracking block 138 from Figure 2 in greater detail. A tracking block 138 comprises a signal power estimation functions block 182, a tracking control block 184, a discriminate function block 186 and a loop filter block 188. The loop filter block 188 is further comprised of simple gain function 190 and third order loop filter function 192. The input samples are received at the signal power estimation functions block 182 and at the discriminate function block 186. The reset signal is received at tracking control block 184. The signal power estimation functions block 182 generates a signal power value (S_P), signal which is sent to AGC block ~~112~~ 116 and a c_max value which is available to the installer as the beacon strength indicator (BSI). In addition to receiving samples, the discriminate function 186 receives early and late versions of the PN sequence from the PN ~~sequency~~ sequence generator 146. The discriminate function compares the incoming samples to both the early and late versions of the PN signal and generates a discriminate function value which is passed either to simple gain block 190 or third order loop filter block 192. The functionality of the discriminate function block 186 will be described in greater detail below. Simple gain block 190 or third order loop filter block 192 are alternatively enabled by a filter flag signal (Flag_filter) supplied by tracking control block 184. The output of loop filter block 188 is a VCO frequency offset value (f_{VCO}) that is sent to mode switch ~~42~~ 142 and from there on to the VCO to adjust the VCO frequency.

Please replace Paragraph No. 61 (page 15) with the following:

[0061] The DRO frequency offset estimator and lock detector 134 of Figure 2 is shown in greater detail in Figure 12. In the DRO frequency offset estimator and lock detector 134 the received input samples are multiplied at multiplier 226 with samples representing an on-time PN sequence received from PN

sequence generator 146. A series of samples representing the product of the on-time PN sequence with the received samples is output from multiplier 226 and sent to decimator 228. The decimator 228 decimates the number of samples in the received product sequence and outputs a decimated sequence (d[n]) to a 128 point FFT block 230. The output of the 128 FFT block 130 is 128 indexed values (y[i]) representing the magnitudes of 128 frequency components generated from the decimated input samples. The 128 frequency component magnitude values are generated in each of the 128 frequency bins of the 128 FFT block ~~130~~ 230.

Please replace Paragraph No. 62 (page 16) with the following:

[0062] The lock detector 232 receives the 128 frequency component magnitude values and generates a lock flag (flag_lock) and a maximum index value, i_max. The maximum index is the index number of the maximum value frequency component from FFT block ~~130~~ 230. The lock flag indicates whether or not the incoming signal is locked with the on-time PN signal. The lock flag is then sent to both a frequency estimator 234 and mode selection control block 140. The value i_max is also sent to the frequency estimator 234. The frequency estimator block 234 receives the maximum index value, i_max and the lock flag and determines an NCO frequency offset value to be sent to the frequency control block 148. The NCO frequency offset value, f_{NCO2} will be used to adjust the frequency of the NCO in the NCO and control logic block 128.

Please replace Paragraph No. 66 (page 18) with the following:

[0066] During the initial frequency acquisition and unique word lock confirmation steps, the entire 3 msec of each downlink frame is tested for the presence of the unique word. Also, during this period the gain of the AGC 116 is determined based on the peak power received during any ½ time slot interval during each frame. If the unique word lock confirmation step 252 passes, acquisition

continues with the initial time acquisition step 254. After the initial time acquisition 254, the acquisition integrity is tested at step 256. If the acquisition integrity test passes, the system begins a PN phase search and an initial ~~VCR~~ VCO frequency offset reduction at step 258. If at any time the acquisition integrity fails, the frequency acquisition step 250 must be repeated. Otherwise, the system continues to search for the PN phase and to reduce the initial VCO frequency offset.

Please replace Paragraph No. 68 (page 18) with the following:

[0068] The steps performed during acquisition mode are described more fully in Figure 16. The first step is frequency acquisition and UW lock confirmation 264. During this step, an acquisition flag, flag_aq, is set once the frequency and unique word lock confirmation has been completed. This process is described in more detail below. The acquisition flag is tested at step 266, and if it has not been set, then the frequency of the NCO is adjusted at step 268 and the frequency acquisition and unique lock confirmation step 264 continues. If the acquisition flag has been set, however, the beacon demodulator ~~110~~ 112 begins two parallel processes. The first process consists of an initial timing acquisition step 270, a coarse VCO frequency pull-up step 272 and an adjust VCO step 274. The second parallel process consists of a generate local PN sequence step 276, a DRO frequency offset estimator and lock detector step 278 and an adjust NCO frequency step 280. During the two parallel processes, a pull-up flag, flag_pull and a lock detection flag, flag_lock, are either set or not set depending on whether the VCO frequency has been pulled up to within tolerance and whether the system has locked onto the PN sequence. The mode selection control block 142 tests the lock detection flag and the pull-up flag at step 282. Once both flags have been set, the system moves to the tracking mode. If either the lock detection flag or the pull-up flag are not set then the system continues in the acquisition mode.